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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,709	07/28/2003	Yoshio Hirose	1448.1041	7098

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,709	HIROSE ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 and 12-24 is/are rejected.

7)☒ Claim(s) 9-11 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-8,13,15-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato (patent No. 6,826,674).

4. Sato taught the invention as claimed including a data processing ("DP") system comprising (as per claims 1,16):

a) Deciding unit (42)(and steps therefore) that decides whether a given instruction exists within a predetermined instruction set (e.g., see figs. 1,11 and col. 11, line 5-col. 12, line 4) [fetch unit decodes general purpose instructions of a predetermined instruction set and decoder (in a separate decoder) data flow designating instructions from a single program (41) fetched from code RAM 39. Therefore, inherently the fetch unit (or some means associated with the fetch unit) must have determined which instructions were general purpose instructions and which

instructions were data flow instructions so the respective instructions could be sent the appropriate dedicated decoder];

b) First operating unit (43)(and steps therefore) that executes the instruction when the deciding unit decides that the instruction exists within the predetermined instruction set (e.g., see col. 11, lines 39-47);

b) Structure information output unit (62y)(and steps therefore) that outputs structure information for determining a circuit structure to execute the instruction when the deciding unit decides that the instruction does not exist within the predetermined instruction set (e.g., see fig. 13 and; and col. 13, lines 1-46)[output from decoder is input to configuration register and configuration RAM in figure 13];

d) Second operating unit (plural DPU units 46)(and steps therefore) that executes the instruction in the circuit structure determined based on the structure information output from the structure information output unit (e.g., see col. 11, lines 47-58).

5. As per claim 2 Sato taught the second operating units (46) were provided in plurality (e.g., see col. 11, line 38-col. 12, line 41).

6. As per claims 3,17 Sato taught when the deciding unit decides the instruction does not exist within the predetermined instruction set (general purpose instruction set), the structure information output unit selectively outputs structure information for determining the circuit structure to execute the instruction, from among pieces of structure information (e.g., see fig. 11 and col. 15, lines 34-61);

7. As per claims 4,18 Sato taught the structure information (62y) output unit selectively outputs structure information for determining the circuit structure to execute

the instruction from among the structure information, based on any one of an address assigned by the instruction and an address held in an predetermined register or both e.g., see fig. 13 and col. 13, lines 6-25).

8. As to claim 5,19 Sato taught rewriteable memory (CRAM 76) for storing the structure information (e.g., see fig. 13 and col. 15, lines 36-62).

9. As per claims 6,20 Sato taught wherein addition to the memory (76) the structure information is stored in a predetermined field of the instruction or in a predetermined register (configuration register 75) (e.g., see fig. 13, and col. 15, lines 36-62).

10. As per claims 7,21 Sato taught each time the second operating unit executes the instruction, a value held in the predetermined register (75) is updated based on the structured information held in the memory (76) (e.g., see col. 16, lines 41-62).

11. As per claims 8,22,23 Sato taught the instruction (that is issued for execution) includes an instruction that instructs to load the structure information into the memory (e.g., see col. 9, lines 22-37 and fig. 13)[the instruction comprise a move instruction for moving data to the destination and in fig. 13 the destination is the configuration RAM 76 and configuration register 75].

12. As per claim 13, Sato taught the second operating unit replaces optional bits within given data, the circuit structure determined based on the structure information output from the structure information output unit(e.g., see fig. 8 and col. 6, lines 7-67 and col. 9, lines 22-59).

13. As per claim 15,24 Sato taught selecting unit (71) that outputs only information at a predetermined bit position within the structure information output from the structure

information output unit (e.g., see fig. 15)[only predetermined bit positions from the data stored in the configuration register that was output from the structure information output unit as described above are output)(e.g., see col. 13, line 63-col. 14, line 65).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (patent No. 6,826,674).

16. Sato taught the invention as claimed including a data processing ("DP") system comprising:

a) Deciding unit (42) that decides whether a given instruction exists within a predetermined instruction set (e.g., see figs. 1,11 and col. 11, line 5-col. 12, line 4) [fetch unit decodes general purpose instructions of a predetermined instruction set and decoder (in a separate decoder) data flow designating instructions from a single program (41) fetched from code RAM 39. Therefore, inherently the fetch unit (or some means associated with the fetch unit) must have determined which instructions were general purpose instructions and which instructions were data flow instructions so the respective instructions could be sent the appropriate dedicated decoder];

b) First operating unit (43) that executes the instruction when the deciding unit decides that the instruction exists within the predetermined instruction set (e.g., see col. 11, lines 39-47);

b) Structure information output unit (62y) that outputs structure information for determining a circuit structure to execute the instruction when the deciding unit decides that the instruction does not exist within the predetermined instruction set (e.g., see fig. 13 and; and col. 13, lines 1-46)[output from decoder is input to configuration register and configuration RAM in figure 13];

d) Second operating unit (plural DPU units 46) that executes the instruction in the circuit structure determined based on the structure information output from the structure information output unit (e.g., see col. 11, lines 47-58).

17. As per claim 12, Sato taught a decoder that performs the operation of deciding whether the instruction decoded is an instruction to load the structure information into memory (CRAM) when the deciding unit decides that instruction does not exist within the predetermined instruction unit (e.g., see fig.13 and col. 7, lines 34-45, and col. 13, lines 6-46).Sato also taught performing DMA transfer of data using data from the "Y" field of the instruction that determined where the configuration or structure data was to be stored (e.g., see col. 6 lines 30-67). Therefore the function of instructing the system to store the configuration in memory using DMA was within the scope of the Sato teachings. One of ordinary skill would have been motivated to use a DMA controller for perform the DMA operation at least to provide efficient DMA operation.

18. As per claim 14, Sato did not expressly detail the second operating unit counts 1s within a given data, in the circuit structure determined based on the structure information output from the structure output unit. However since Sato taught configuration of plural units of selectively executing instruction one of ordinary skill would have been motivated to count 1s in a given data at least to account for the processing completion each of the processors[by counting completion signals and comparing the number of completion signals (such as 1s stored in a status register) to the number of processors that was participating in processing the system could determine if the combined processing was completed].

Allowable Subject Matter

19. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Studor (patent No. 5,848,289) disclosed a extensible central processing unit (e.g., see abstract).

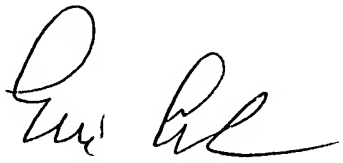
Pechanek (patent No. 6,128,720) disclosed a distributed processing array with component processors performing customized interpretation of instructions (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN
PRIMARY EXAMINER